Amendments to the Specification:

Page 3, please replace the paragraphs spanning page lines 5-26 as follows:

To achieve the above-described object of the present invention, according to the present invention, there is provided a delay apparatus for delaying a digital signal for a predetermined delay period of time, the digital signal having [[a]] first and [[a]] second logic levels, comprising:

a first edge detection circuit which detects a first edge of the digital signal whereon the level of the digital signal changes from the first logic level to the second logic level, and generates a first detection signal;

a set circuit which includes a first counter for counting a reference clock signal to generate a count value and clearing its own count value in response to the first detection signal, wherein the set circuit generates a set signal if the count value reaches the number of the reference clock signals corresponding to the delay period of time;

a reset circuit which generates a reset signal if an elapsed period of time since a generation of the set signal equals ~~to~~ a period of time while the digital signal ~~maintain~~ maintains the second logic level; and

an output circuit which outputs a digital signal including edges synchronized with the set signal and the reset signal.

Page 9, please replace the paragraph spanning page lines 4-16 as follows:

As shown in FIG. 2, the mode set signal H (H="16") is input to the decoder 8 via the input terminal 9. The decoder 8 outputs the address value I (I="8") based on the interpreted number of the clock pulse signal C. The storage circuit 7 outputs the output signal ~~E~~ G the value of which is equal to "8", stored at an address of "8". As described above, the setting of the number of the clock pulse signals C corresponding to the delay period of time T is performed. The storage circuit 12 stores the number of clock pulse signals C corresponding to the delay period of time T as "6" in advance. The values of the mode set signal H and the address value I are just one example. Various values can be applied to the system the delay apparatus of the present invention is used.

Page 21, please replace the paragraph spanning page 21, line 22 through page 22, line 13 as follows:

In FIG. 7, the delay apparatus 41 of the fourth embodiment of the present invention comprises a rising edge detection circuit ~~42~~ 43 and a falling edge detection circuit ~~43~~ 42. Each edge detection circuit 42 and 43 is constituted in the same manner as the edge detection circuit 4 and 23 described above. Each edge detection signal D and D' is connected to an OR circuit 44. An output signal K of the OR circuit 44 is connected to an write address counter 46. The write address counter 46 increments ~~an~~ a write address WA in response to the output signal K of the OR circuit. The write address counter 46 resets the write address WA at "0" in response to a system reset signal RST input from outside via a reset terminal 45. If the write address WA reaches the countable maximum address, the write address counter 46 begins to increment the write address WA from "0" once more. In the fourth embodiment, the countable maximum address is set at "3". The write address WA output from the write address counter 46 is connected to a storage circuit 47. The write address counter 46 also outputs the least significant bit (LSB) of the write address WA to a selector 48 described later. The LSB of the write address WA is showed by symbol LSB1 in FIG. 7.